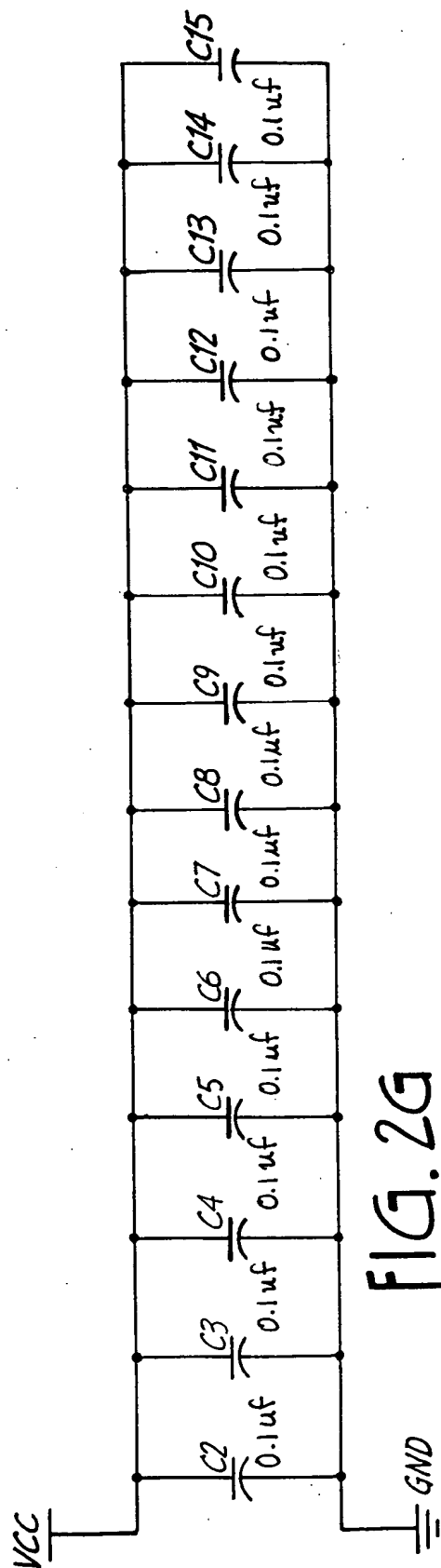


FIG. 1

FIG. 2A	FIG. 2B	FIG. 2C
FIG. 2D	FIG. 2E	FIG. 2F
FIG. 2G		

FIG. 2



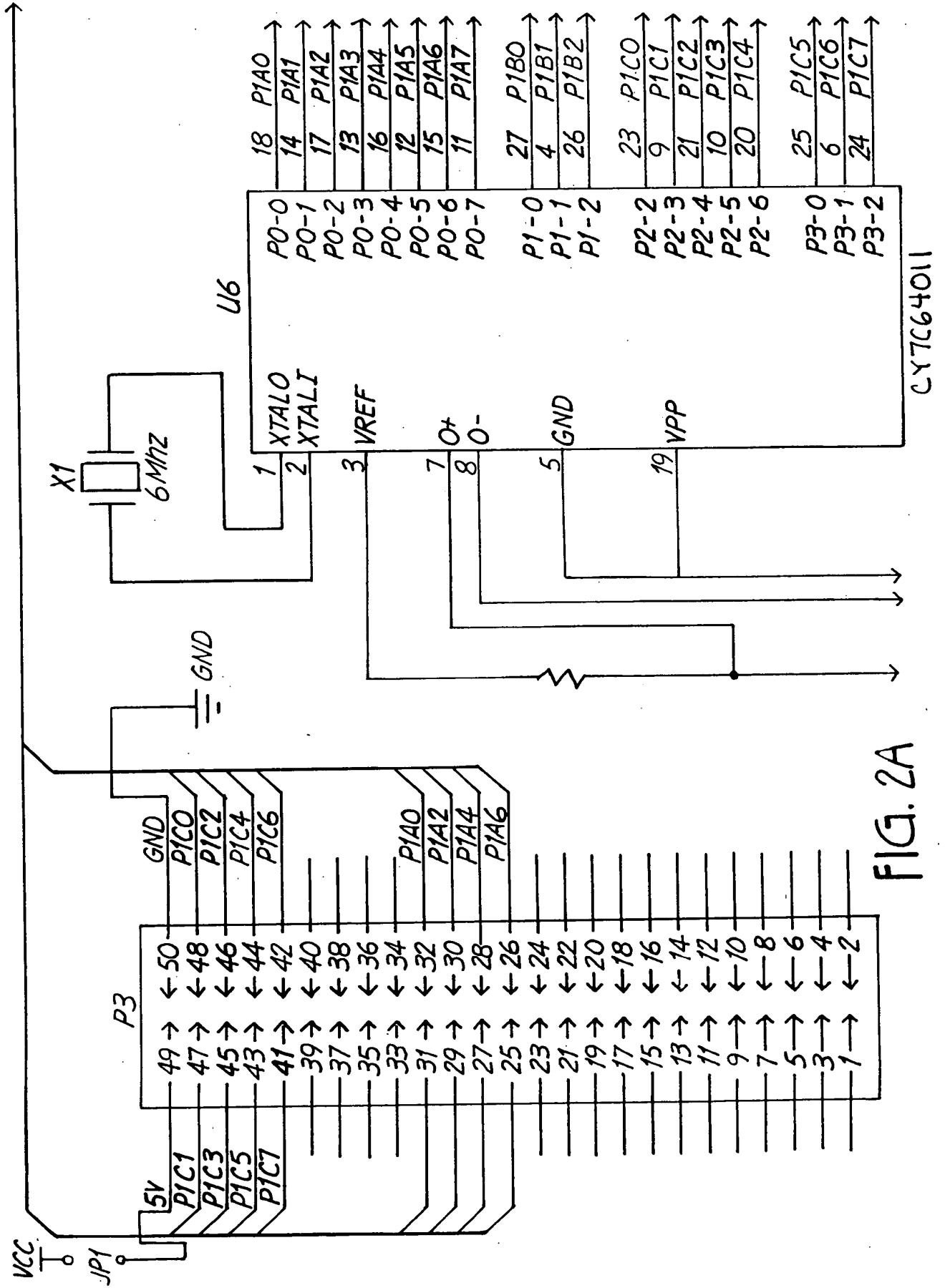


FIG. 2A

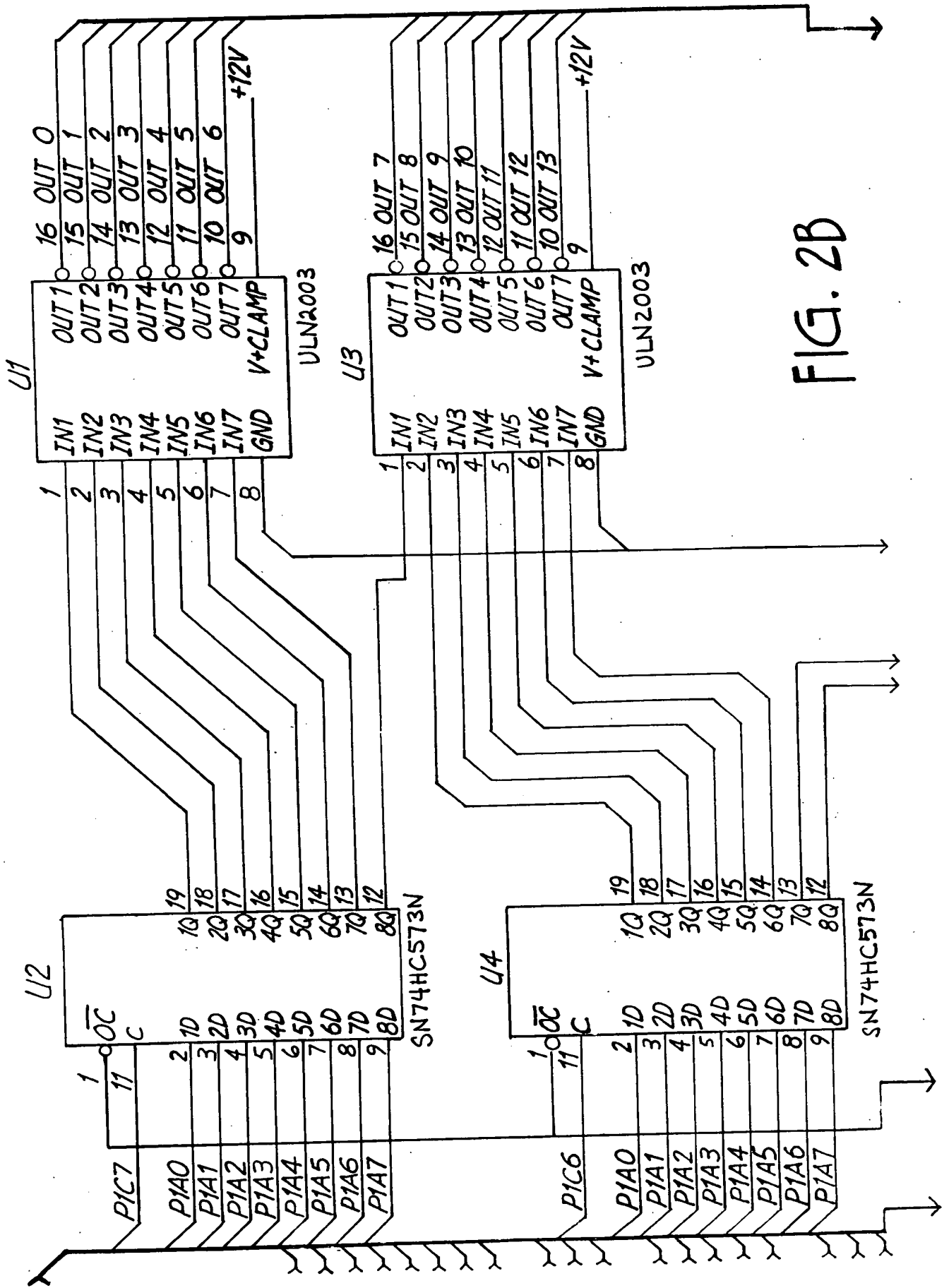


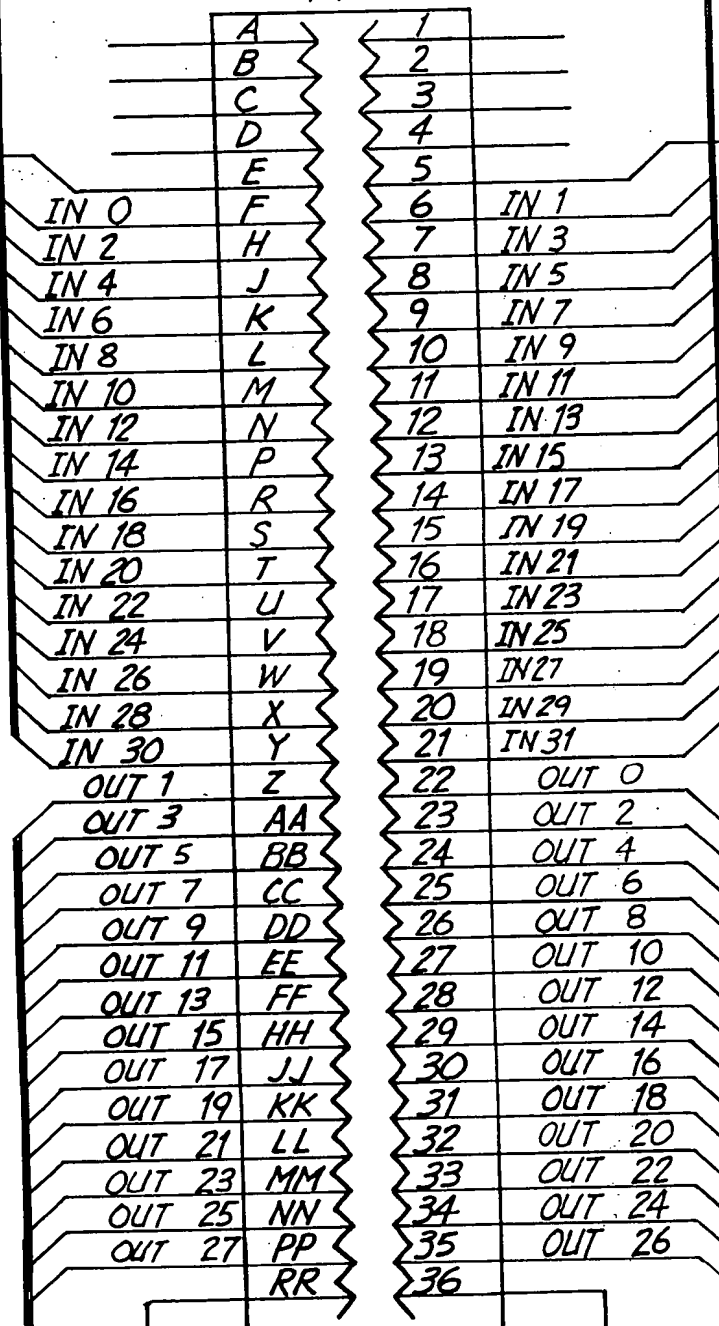
FIG. 2B

IN 0 - IN 31

P1

SPKR R+

SPKR R-



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FIG. 2C

FIG. 2C

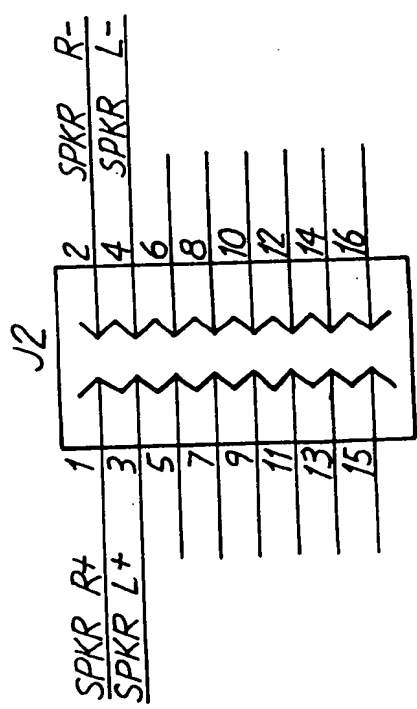
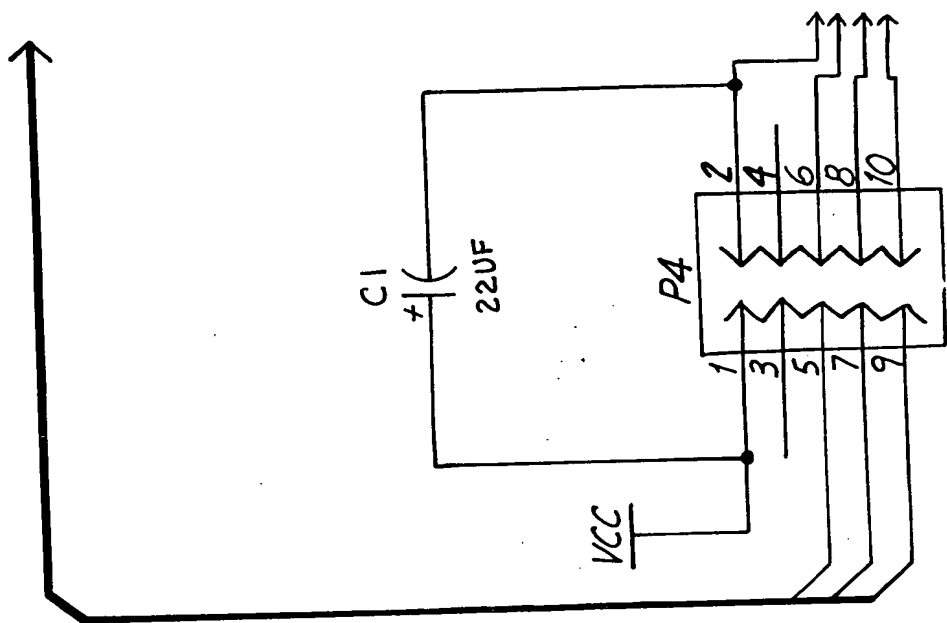
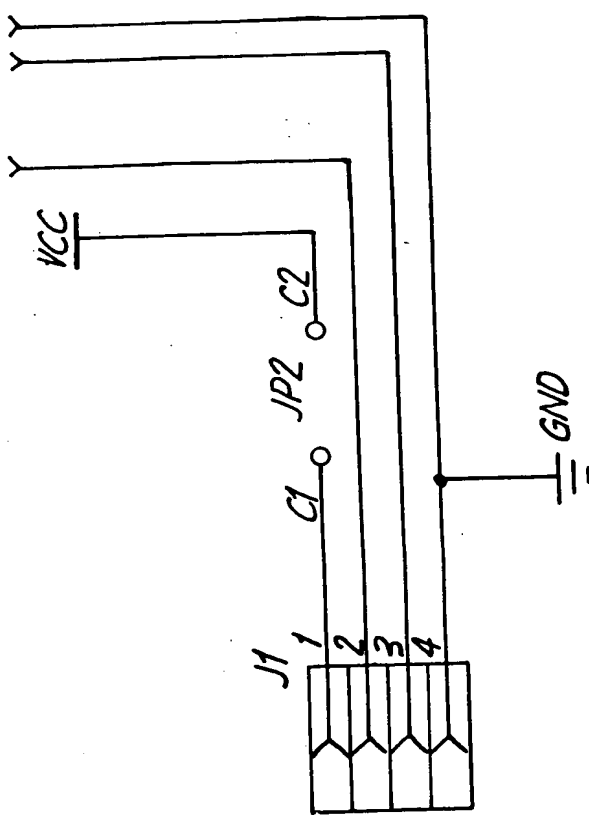


FIG. 2D

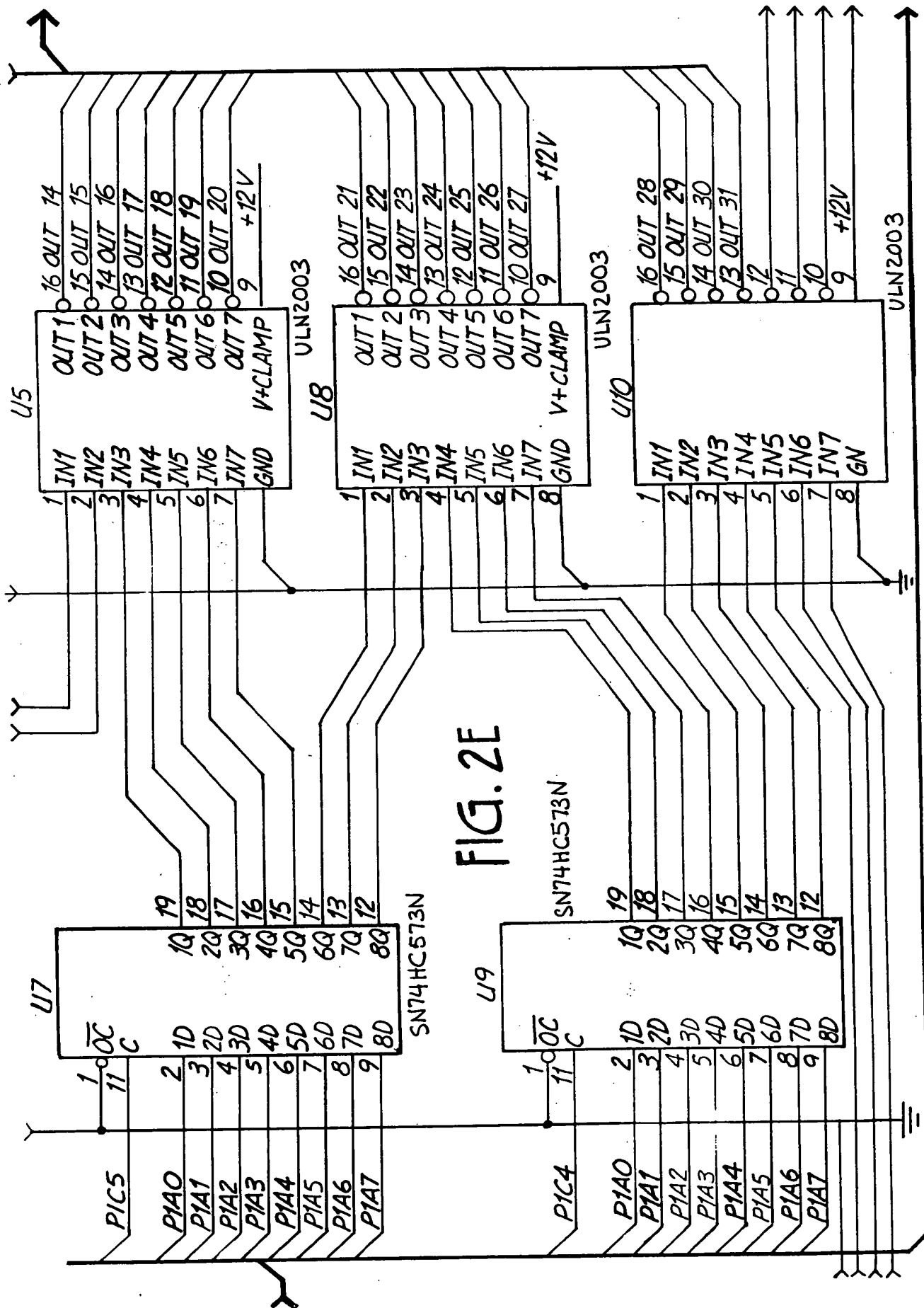
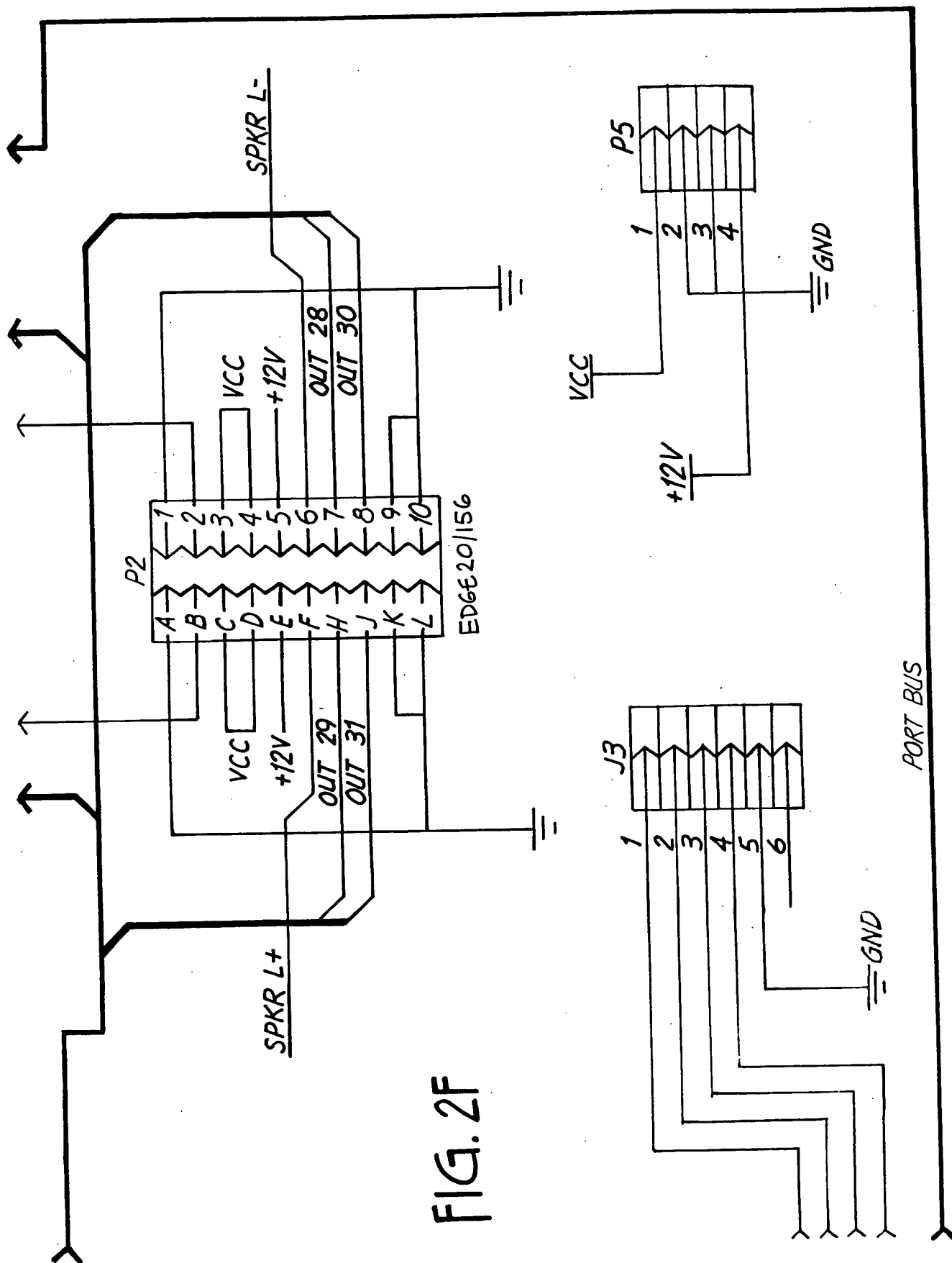


FIG. 2E



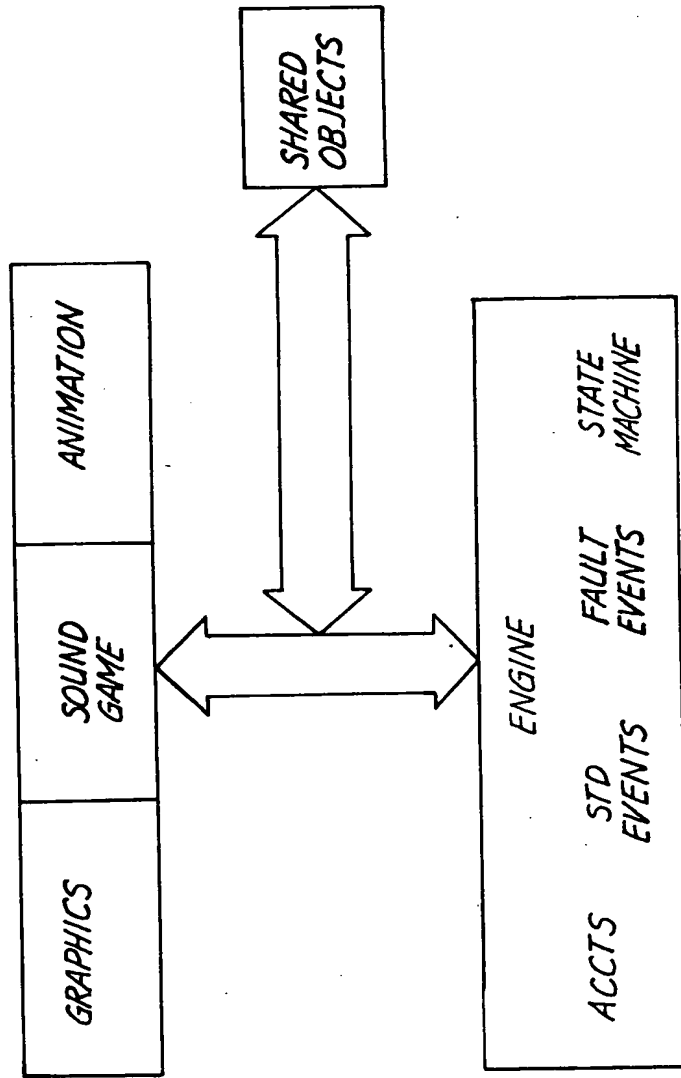


FIG. 3

GRAPHICS	I/O	TIMER	SOUND	NV RAM
EVENT LOOP				

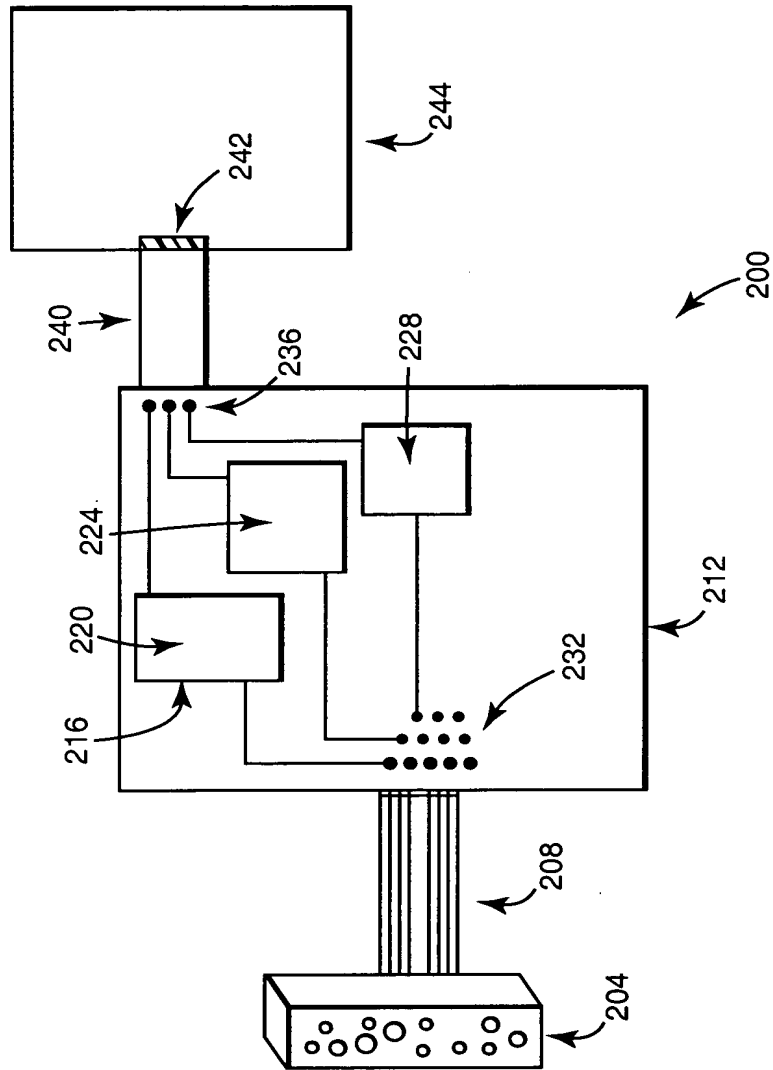


Fig. 4

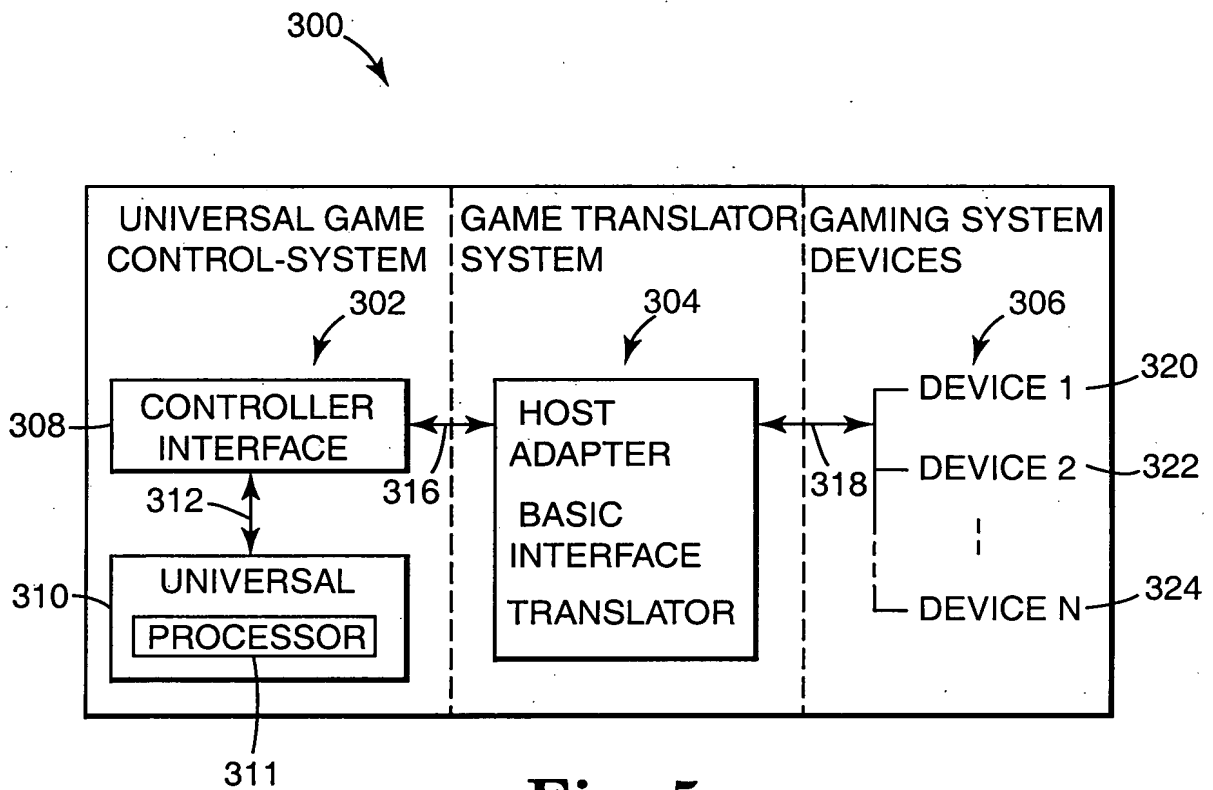


Fig. 5

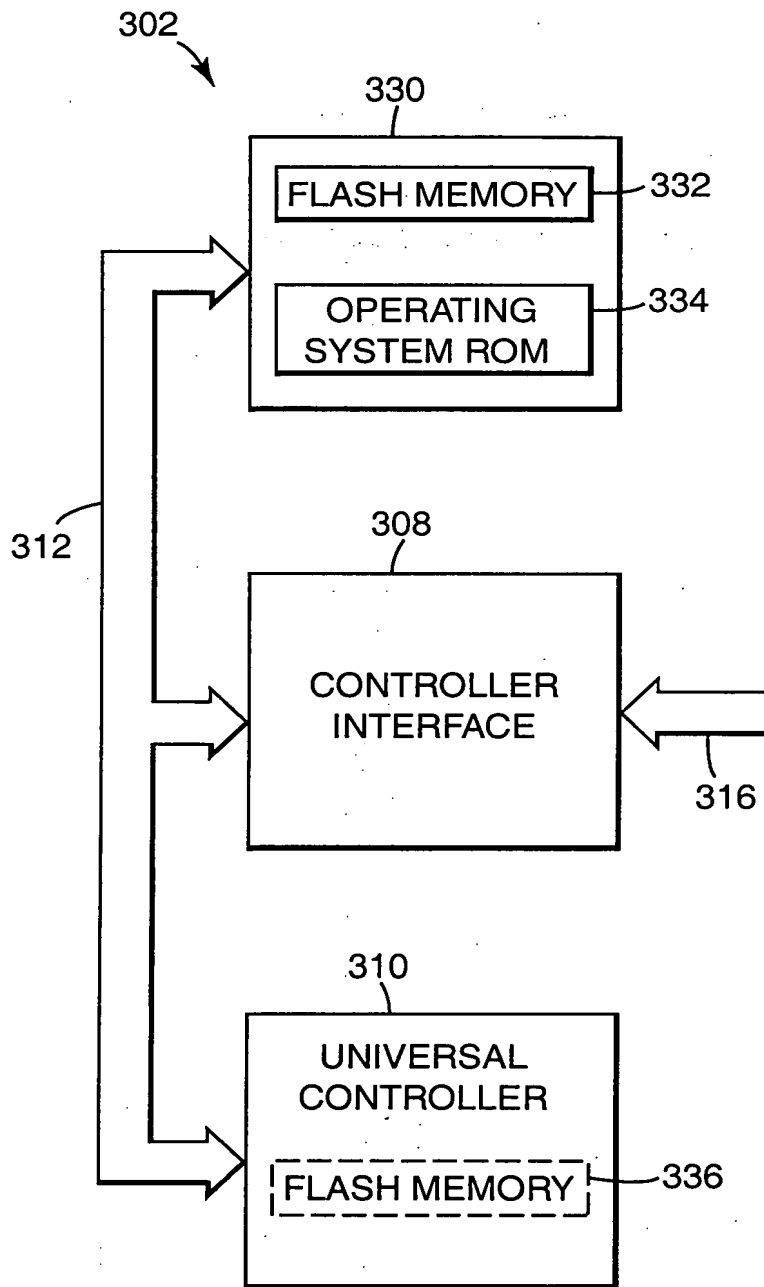


Fig. 6

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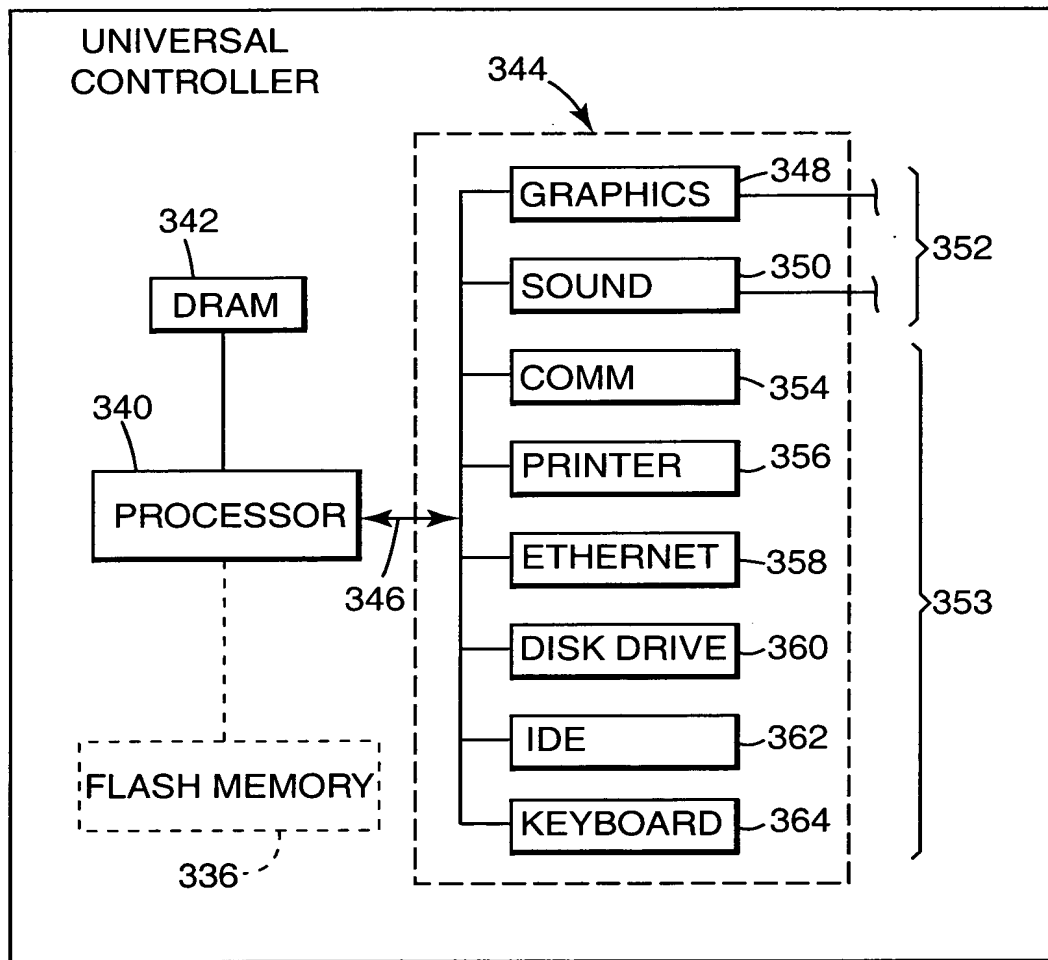


Fig. 7

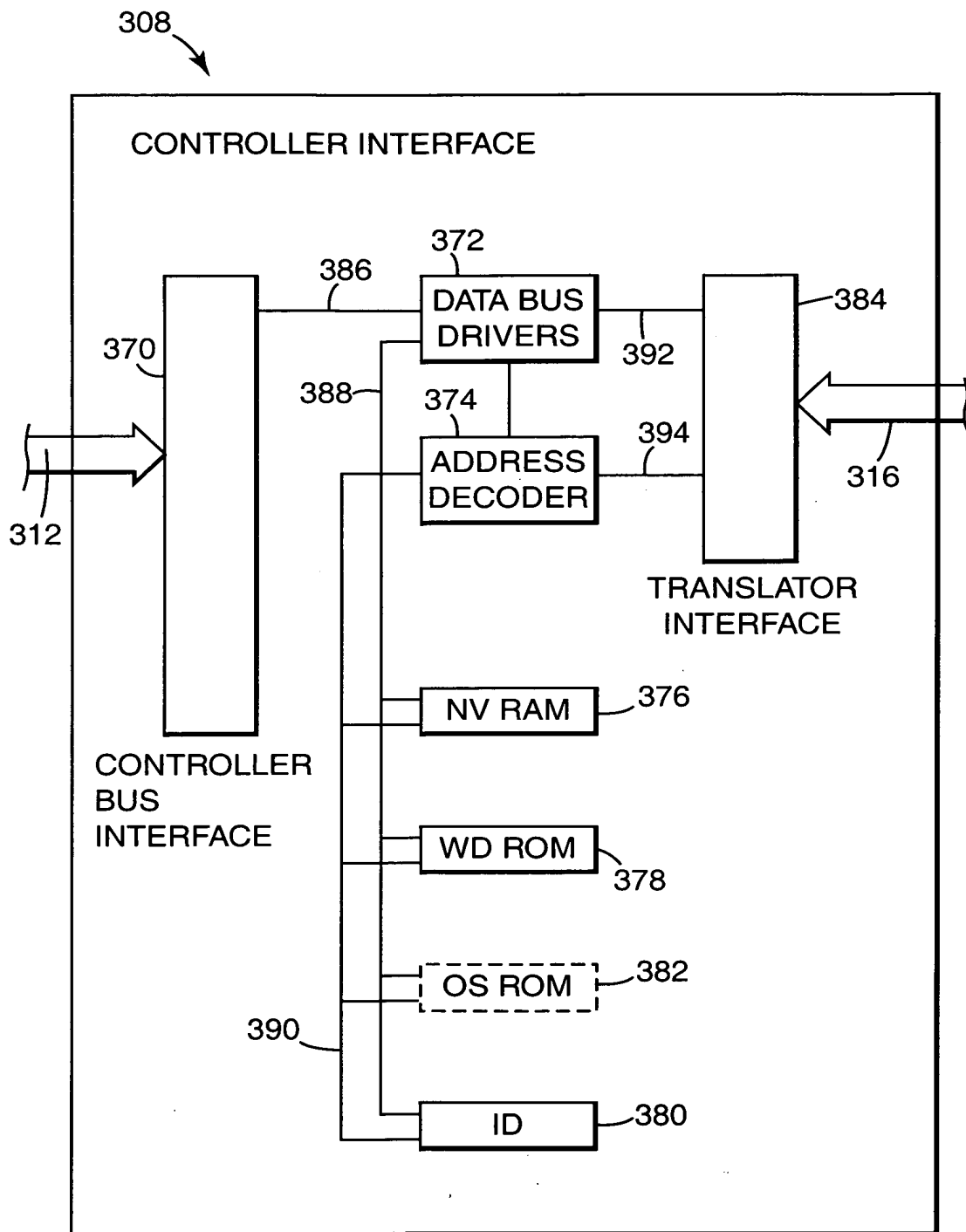


Fig. 8

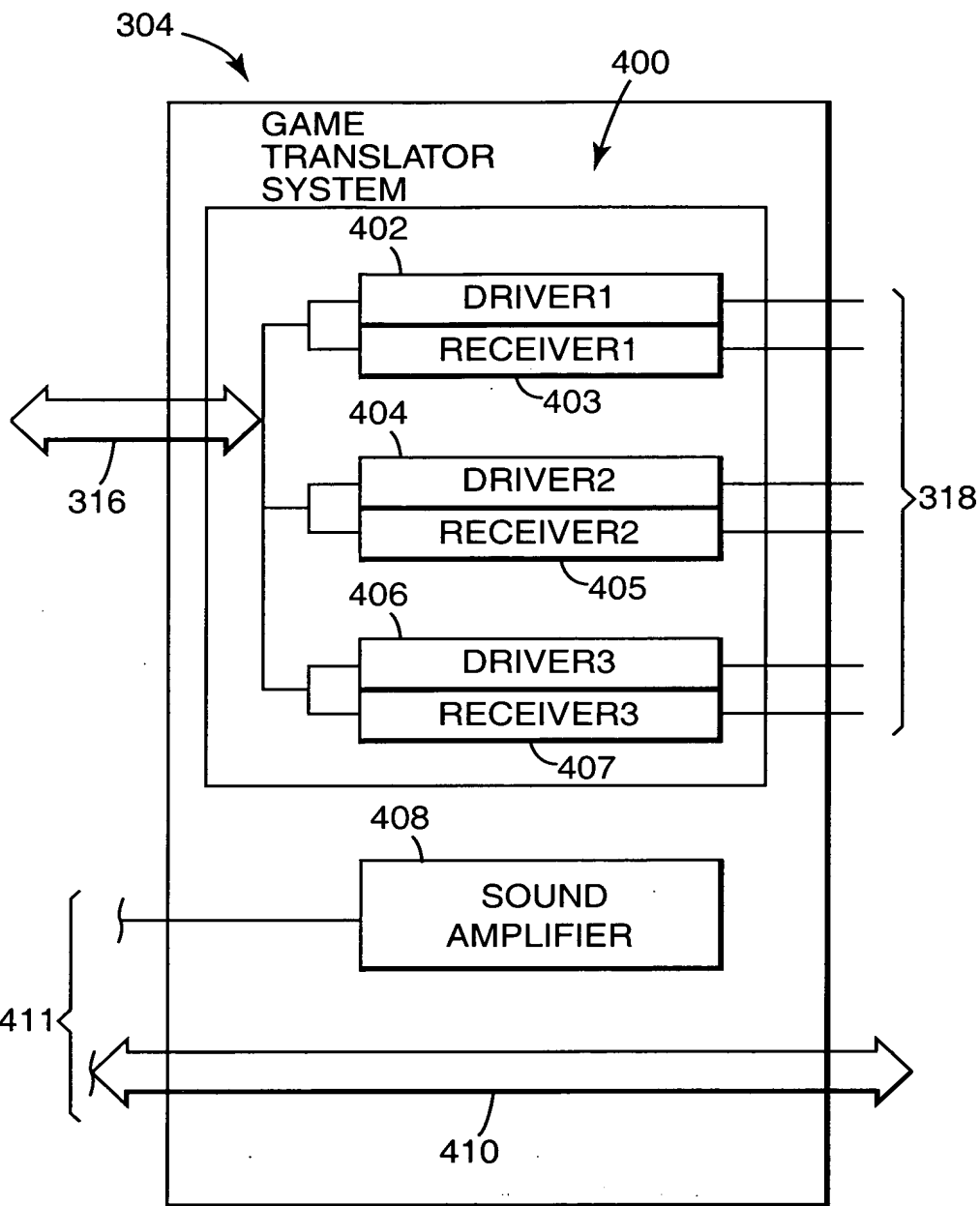


Fig. 9

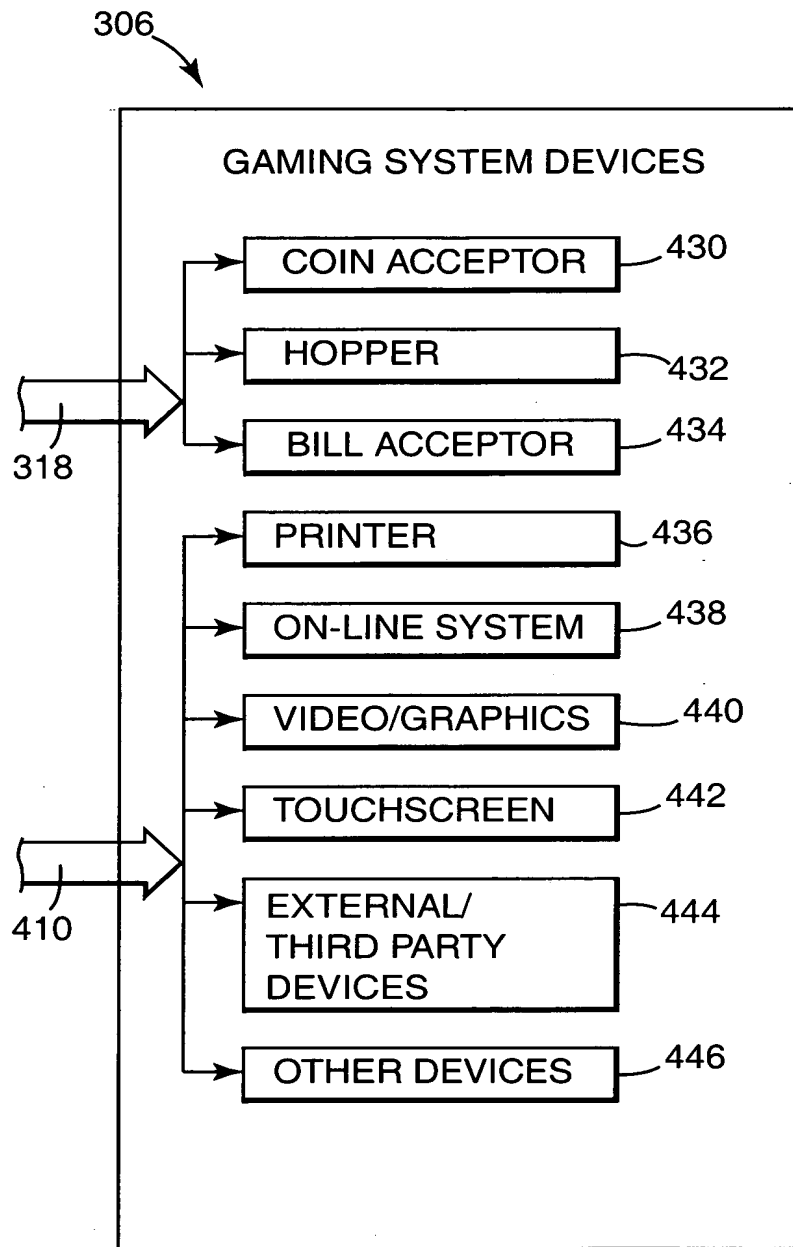


Fig. 10

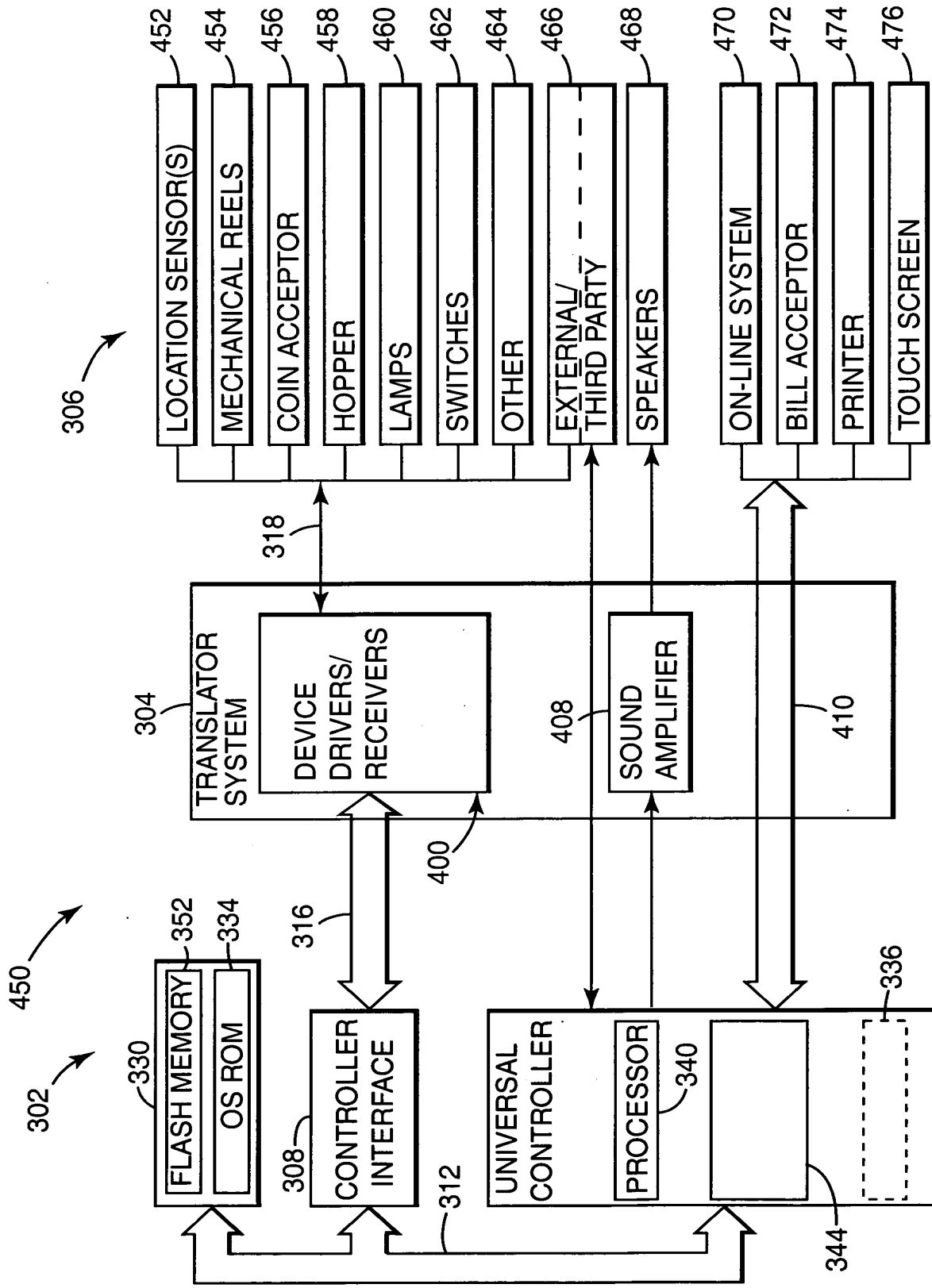


Fig. 11

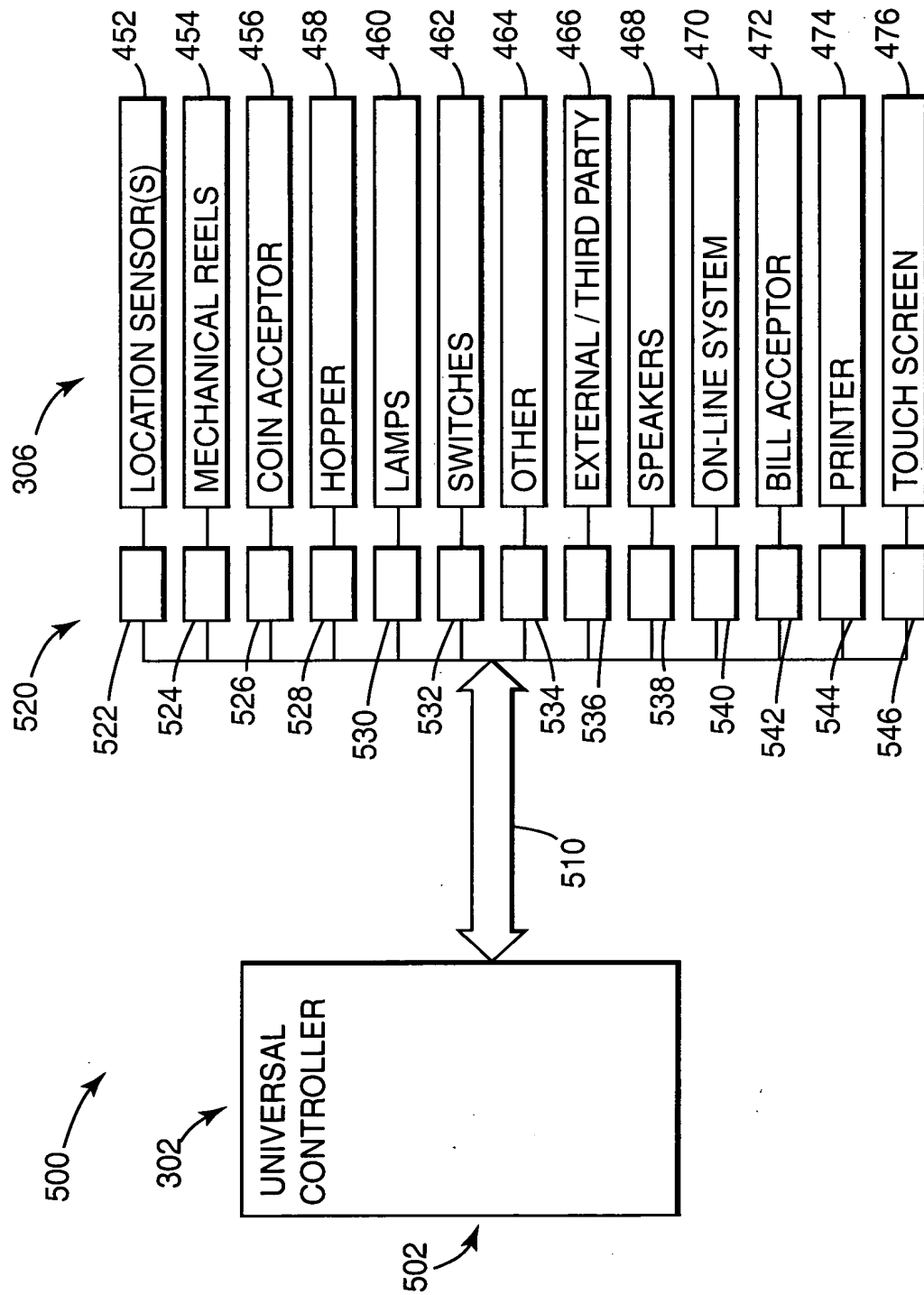


Fig. 12